

# IBM-PC Parallel Printer Port Programming Considerations

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## Please Note:

I got this information from original technical documentation, but I am informed by Steve Walz <[rsteve@armory.com](mailto:rsteve@armory.com)> that it contains a number of inaccuracies. His provided annotations are [here](#)

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The printer adapter responds to five I/O instructions: two output and three input. The output instructions transfer data into two latches whose outputs are presented on the pins of a 25-pin D-type female connector.

Two of the three input instructions allow the processor to read back the contents of the two latches. The third allows the processor to read the realtime status of a group of pins on the connector.

A description of each instruction follows

## Output to address 278/378/3BC Hex

Bit	7	6	5	4	3	2	1	0
Pin	9	8	7	6	5	4	3	2

The instruction captures data from the data bus and is present on the respective pins. These pins are each capable of sourcing 2.6 mA and sinking 24 mA. It is **essential** that the external device not try to pull these lines to ground.

## Output to address 27A/37A/3BE Hex

Bit	7	6	5	4	~3	2	~1	~0
Pin	-	-	-	IRQ	17	16	14	1
				enable				

This instruction causes the latch to capture the least significant bits of the data bus. The four least significant bits present their outputs, or inverted versions of their outputs, to the respective pins shown above. If bit 4 is written as 1, the card will interrupt the processor on the condition that pin 10 transitions high to low.

These pins are driven by open collector drivers pulled to +5 Vdc through 4.7 k-ohm resistors. They can each sink approximately 7 mA and maintain 0.8 volts down-level.

## Input from address 278/378/3BC Hex

This command presents the processor with data present on the pins associated with the corresponding output address. This should normally reflect the exact value that was last written. If an external device should be driving data on these pins (in violation of usage groundrules) at the time of an input, this data will be ORed with the latch contents.

**Input from address 279/379/3BD Hex**

This command presents realtime status to the processor from the pins as follows.

Bit	7	6	5	4	3	2	1	0
Pin	11	10	12	13	15	-	-	-

**Input from address 27A/37A/3BE Hex**

This instruction causes the data present on pins 1, 14, 16, 17 and the IRQ bit to be read by the processor. In the absence of external drive applied to these pins, data read by the processor will exactly match data last written to the corresponding output address in the same bit positions. Note that data bits 0-2 are not included. If external drivers are dotted to these pins, that data will be ORed with data applied to the pins by the output latch.

Bit	7	6	5	4	3	2	1	0
Pin	-	-	-	IRQ	~17	16	~14	~1

enable

state assumed after processor reset

0 1 0 1 1

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